Research Result

Design A 8-bit Successive Approximation Register (SAR) ADC for High Resolution Rate

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ABSTRACT

In this paper, we have done research on SAR ADCs data converters are commonly used, but their use is limited to low-speed applications and high-resolution bits. This is due to the inherent limitation in the implementation of ADC SAR. It typically offers 8-to-18-bit resolution with a sampling rate below 40 Msps, making it ideal for applications such as data acquisition, battery powered tools, industrial commands, etc. This limits the maximum sampling rate that can be operated and accurate resolutions of output waveforms. This document describes a new SAR-ADC-based architecture that goes beyond this implementation limit. We call it the Successive Approximations register ADC. This thesis presents execution of a 8 bit SAR ADC working at 330 MS/s and supply voltage of 3 V.

KEYWORDS

Successive approximation register (SAR), Analog to digital Converter (ADC), Digital to Analog converter (DAC), MATLAB software, Conversion Speed

1. INTRODUCTION

During the 1940s and 1950s, the electronics market demanded analog-to-digital conversion devices. For this reason, data converters have become a need in the industry, especially in the field of communication [1].

In the field of electronics, analog-to-digital converters (ADCs, A-to-D or A / D) are responsible to convert analog signals (e.g., audio signals recorded by a microphone, visible spectrum entered into the digital camera, etc.) into digital signals.

The ADC can also provide remote measurements in the form of an electronic devices which converts

into an analog input or current voltage into a

numerical value that indicates the magnitude value of the voltage or current. Successive approximation

ADC is best for the low and medium costs

resolution applications [2]. The resolution for SAR

ADCs goes from 8 to 18 bits, with sample range up to 5 mega samples per second (Msps). In addition, it can be manufactured in a small factor with low power consumption and that is why this type of ADC is used for battery consumption portable devices. For high demands, there is a better deal of concern about the speed and resolution of ADC.

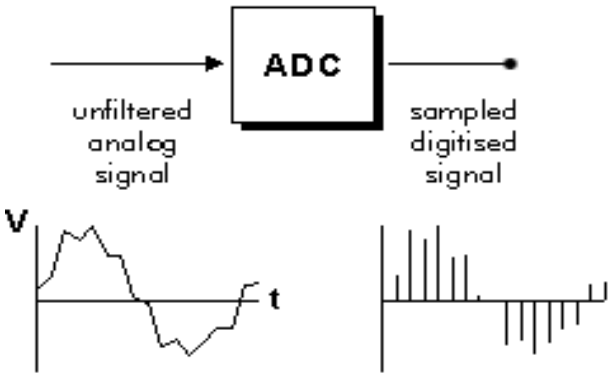


Fig.1 Analog to digital converter (ADC)

The main function of an ADC in a Data acquisition system is to convert the received analog signal into a digital data stream so that the data acquisition system can process it for display, storage and analysis. There are the types of ADCs below:

Successive Approximation (SAR) ADC

Delta-sigma (ΔΣ) ADC

Dual Slope ADC

Pipelined ADC

Flash ADC

1.1 Successive Approximation Resistor (SAR) ADC

The world of DAC and ADC is the analog-to-digital (ADC) converter SAR (serial convergence program). It gives the absolute balance of speed and resolution and processes a variety of signals with great accuracy. As it is being used for a long period of time, the SAR design is durable and reliable, the "chip" however, is relatively inexpensive. Consecutive ADC approximation is a type of analog to digital converter that transform a continuous analog wave form to a discrete digital waveform by using binary search through all probable quantification levels before it is converted into digital output for each step of conversion [5].

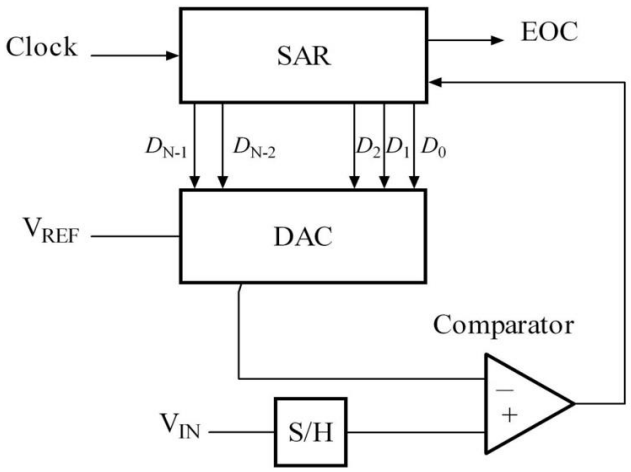


Fig. 2 Typical SAR schematic

1.2 Algorithm of successive approximation

This is an iterative algorithm based on binary search. it works as follows-

The analog input signal is to be converted its corresponding digital output is first compared to the analog equivalent of a digital signal with MSB as 1 (high) and all other bits as 0 (low).

If the input analog signal is larger, the MSB of the digital output signal is set to be 1, or set to be 0. Thus, in the first step, the MSB of the digital output signal is fixed.

In the next step, the same analog input signal is compared to the analog equivalent of the digital signal whose value is set by the MSB to the same value as the MSB of the digital output signal, the second MSB set as 1 and other bits set as a 0.

If the input signal is larger than the volume, the second MSB of the digital-output signal is now set.

Similarly, the above steps are repeated until each bit of the digital out put signal is determined.

Because the SAR algorithm is iterative in nature, the internal components must operate at a much higher frequency than the frequency of the input clock signal.

This high frequency has a very-high resolution +1 times higher and is generated by the clock generator. This is the major problem: consequently, the use of SAR ADC is restricted to medium speed and medium resolution conversion operations.

Mathematically, let Vin = x Vref, so x in [-1, 1] is the normalized input voltage. The goal is to digitize x to an accuracy of about 1 / 2n. The algorithm process are as follows:

Initial approximation xo = 0.

ith approximation xi = xi-1 – s (xi-1 - x)/2i .

where, s(x) is the signum-function(sign(x)) (+1 for x ≥ 0, -1 for x < 0). It is followed as mathematical procedure that |x n - x| ≤ 1/2n.

As shown in the above algorithm, a SAR ADC need some methods:

An input voltage source that is Vin.

A reference voltage source (Vref) to normalize the input with Successive approximation ADC.

A DAC is to convert the i th approximation (xi) to a voltage.

A Comparator to perform the function s (xi - x) by comparing the DAC's voltage with the input voltage.

A Register store the output of comparator and apply xi-1 – s (xi-1 - x)/2i.

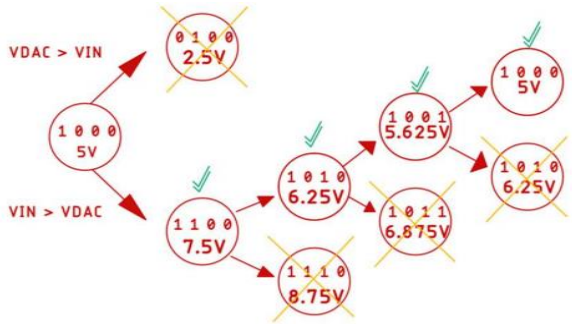


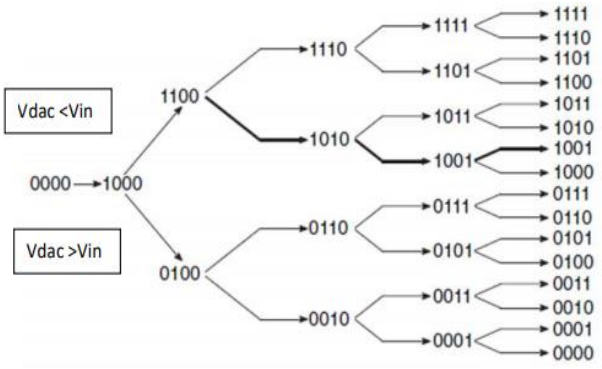
Fig. 3 How ADC converts analog bit into digital format

Thus, the ADC sequential approximation changes 1 bit at a time to determine the input voltage and to produce the output value. Finally, a list of all probable combinations for the four shown below.

1.3 To calculate VDAC for 8-bit DAC:

Example Inputs: Binary (LSB to MSB) = (MSB)1000 0001(LSB), Reference voltage = 5 V, n is taken as 8 as it is 8-bit DAC.

Output: Output analog voltage = 2.529V.



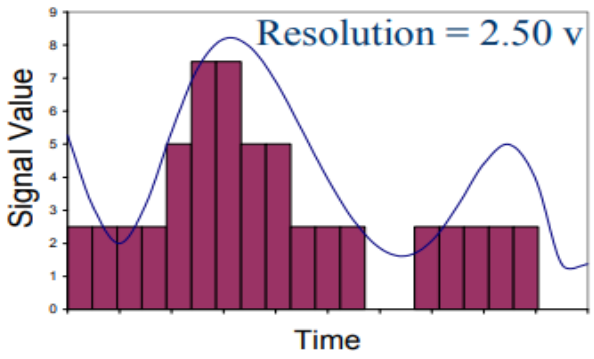


Fig. 4 Resolution when quantized value is 2-bit or 10v/2^2= 2.50v

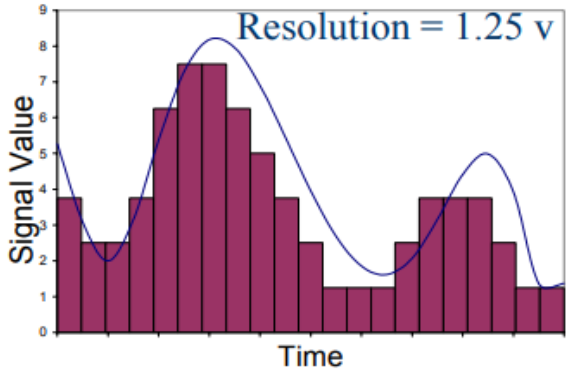


Fig. 5 Resolution when quantized value is 3-bit or

10v/2^3 = 1.25v

1.4 Binary weighted DAC (Digital to Analog converter)

Digital-to-analog converters (DACs) convert digital input signals to analog output signals[6]. Digital signals are represent by a binary code that is a combination of bits 1 and 0. Binary weighted resistor DAC. This is a DAC that converts a particular binary code into an equivalent analog signal. If the binary code specified on the input is constantly changing, so will the output. This type consists of a load resistance (maintained as a multiple of 2) and an inverting and op amp capable of producing a 180-degree phase shift output.

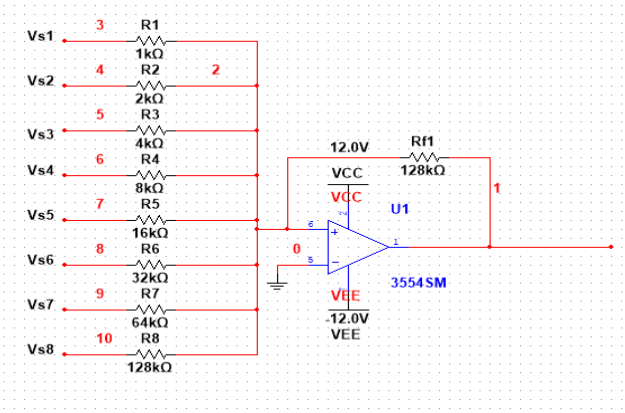


Figure 6: Block diagram of 8-bit binary weighted DAC

2. LITERATURE REVIEW

An analog signal is a continuum of infinite possible values. It is very difficult to process such a signal efficiently, and is practically impossible. Digital signals on the other hand can only have one of two values, i.e., either 0 or 1. This makes them much easier to process and reduces their susceptibility to noise[3]. Alongside these, there are multiple reasons why digital signals are preferred over analog signals. However, since all real signals are analog signals, it is very important to accurately convert these analog signals into an equivalent digital representation. This conversion task is done by a class of devices called ADCs or Analog-to-Digital converters.

The section II-A reviews the Conventional ADC SAR designed with conventional comparator and the section II-B designed with similar comparator reviews the proposed comparator with Successive approximation pipelined ADC[8]. The parameters which are responsible for the performance of ADC are reviewed in section III.

2.1 Conventional SAR ADC scheme

Parallel comparator ADC or 2-bit flash ADC. This is the high speed ADC of all ADC types. The n-bit ADC flash memory requires a comparison (2n-1) and a 2n program[9]. Each comparator starts at Vref = 1/2 (lbs) and compares Vin with a different reference voltage. The operational amplifier is used as a comparator in this case.

2.2 Disadvantages:

It requires many parts, for example, 255 comparators are required for 8-bit ADC. They have lower resolution, comparatively expensive, and are power hungry etc[13].

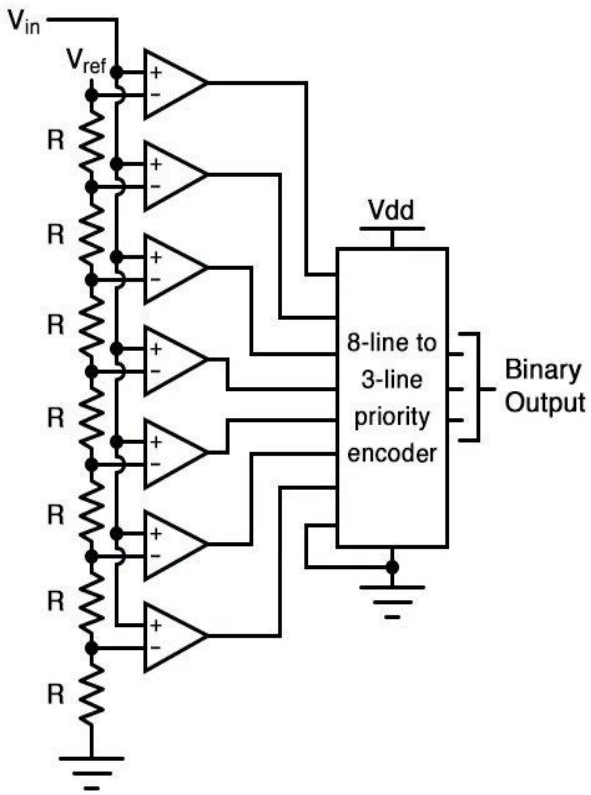


Fig. 7 Parallel comparator (flash ADC)

Proposed SAR ADC

SAR is an abbreviation for Successive Approximation Register. SAR ADCs are primarily used in digital circuits to provide an connection with microprocessors. For SAR

ADCs, the analog voltage conversion times are the same and equal to n * TCLK.

Advantages: It is capable of high speed. It has average accuracy compared to other types of ADCs. In proposed model resolution rate and conversion speed defined:

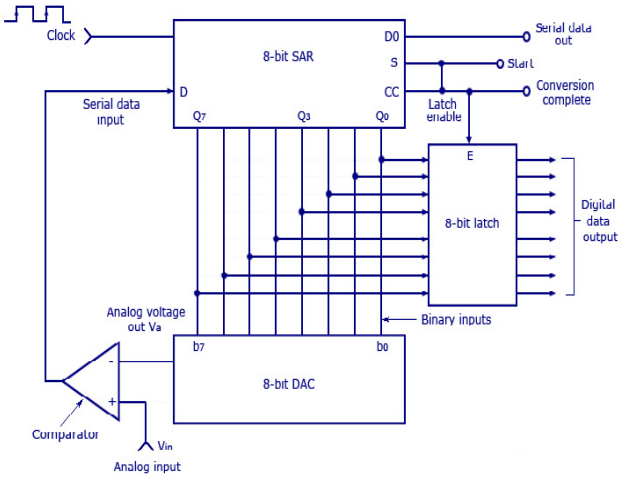


Fig. 8 Proposed SAR ADC schematic diagram

2.3 Resolution Rate:

Converter resolution indicates the number of discrete values that can be output within the range of analog values. The magnitude of the quantization error and hence the maximum possible average "signal to noise ratio" (for an ideal ADC without the use of oversampling) is determined by the resolution [10]. The resolution is generally expressed in bits, as the values are stored in binary format. Therefore, assume that the number of discrete values or "levels" available is a power of two. For instance, an 8-bit ADC can convert an analog input into one of 28 = 256 different levels. The value can represent 0 to 255 (that is, an unsigned integer) or -128 to 127 (that is, a signed integer), depending on the application.

2.4 Conversion Speed

The typical conversion speed of this type of ADC is around 5-10 MSPS (mega samples per second), but there are few ADC which can reach up to 50 MSPS. for a high-speed analog to digital converter, it would be more than 10 msps.

$$TC = N*TCL$$

3. SIMULATION RESULTS

After all the required components are tested individually, they are connected together to form a sequential approximation ADC. An ideal sample & hold circuit is used for resolution and conversion speed.

In order to verify the accuracy first we simulate base paper or previous papers ADC values in our software and check their output results. as some initial specifications are: range of samples =10, no of ADC bits= 4, reference voltage = 5v and input voltage =2v, conversion time for clock time is 2.5us, sampling frequency =190MHz.

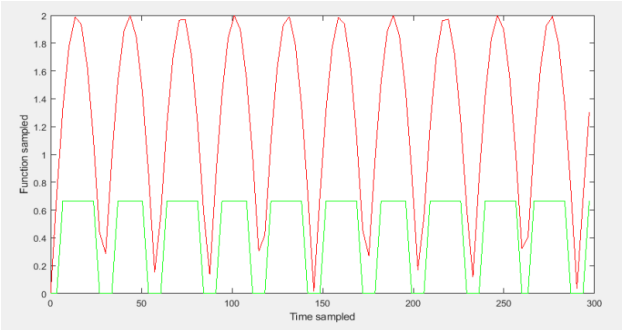


Fig. 9 Output waveform of 4-bit SAR ADC resolution bits

The simulation results of SAR ADC are simply left shifted registers with reference voltage is 5v input voltage is 3v and sampling frequency is around 330MHz[17]. The number of bits of SAR ADC is 8-bit with a clock pulse speed of 2.7ns.

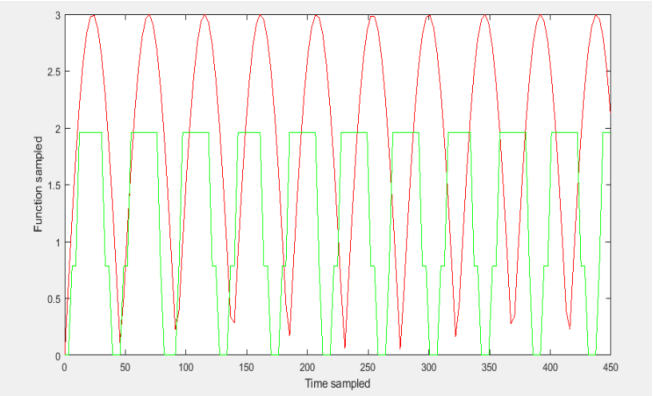


Fig. 10 Final output waveform of successive approximation register

4. CONCLUSION

In this paper, we have done research on SAR ADCs data converters and the design of a new architecture is based on successive approximation algorithms discussed in detail. Its capability of running at a very high sampling rate is explored. An 8-bit SAR ADC is designed is approved for this schematic design. A maximum sampling speed of 330 MHz is achieved. Further directions for exploiting the full capability of this new architecture to achieve 41 msps sampling rate are given. This is just the beginning, possible improvements in future can be expected.

5. FUTURE WORK

Since comparator design is an important part of ADC design, which serves as the main part of the calculation, an efficient comparator is to be designed, for accurate resolution rate with same input bits in such a way to increase the performance of the ADC. In future, more parameter can be analyzed like resolution rate, conversion speed or time conversion rate, power consumption are done and the designs can be further improved to overcome the drawbacks of this structure.

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